Course 8: VLSI Chip Design Hands-on using open source EDA 8th – 12th July 2019

Prospective external Experts: (i) Dr. Imon Mondal, IITK (ii) Prof. Sachin Patkar, IITB, (iii) Dr. Anand Bulusu, IITR (iv) Dr. H. S. Jatana, SCL (v) Dr. Subhakumar Reddy A., VEDA-IIT; (vi) Industry support- VLSI System Design Corp.

Contents of Modules of VLSI Chip Design Hands on using open source EDA

S.No.	Module Name	Topics
1.	**VLSI design, SoC Design**	Generic digital design flow, hierarchical design representation, Platform based SoC design
2.	**Floorplanning & timing analysis**	Floorplanning and pre layout timing analysis [OpenSTA]
3.	**Placement, Clock tree synthesis**	Partitioning, iterative placement, analytical placement, Wire-length estimation; Clock tree synthesis [MAGIC tool]
4.	**Global routing, Detailed routing**	Maze routing, line probe algorithms; Left edge, dog-leg, algorithms; Signal integrity, DRC, LVS, ECO; post layout STA [Orouter, MAGIC tool]
5.	**Analog and Mixed Signal Circuits: Specifications, Design, Layout & GDS**	Important aspects, particular to Analog IC design Flow; Introduction and distinctions between discrete time and continuous time designs; Design of OPAMP, and multi-stage OPAMPs. frequency compensations, noise and non-linearity in a multi-stage OPAMP; Switched capacitor Circuits

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