A Report on Seminar “India’s Techade- Chips for Viksit Bharat@2047” on March 13, 2024

A significant seminar titled "**INDIA’S TECHADE- CHIPS FOR VIKSIT BHARAT@2047**" was held at the **MALAVIYA NATIONAL INSTITUTE OF TECHNOLOGY JAIPUR** to commemorate the importance of India’s Semiconductor Mission to the country’s technological advancement. The event's purpose was to clarify the mission's goals, tactics, and possible effects on India's semiconductor sector.

The seminar featured insightful discussions on various aspects of India's Semiconductor Mission by the Two esteemed experts will grace the seminar: Dr. H. S. Jattana: Former Scientist G/Group Head – Design & Process Group at Semi-Conductor Laboratory, Dept. of Space, Govt. of India, and Dr. Geetha Manjunath: Founder, CEO, and CTO of NIRAMAI Health Analytix.

Emphasis was placed on the mission's objectives, including indigenous semiconductor manufacturing, research and development initiatives, and strategic collaborations. Experts provided valuable insights into the challenges and opportunities associated with building a sustainable semiconductor ecosystem in India.

Summary of activities in workshop on "INDIA’S TECHADE- CHIPS FOR VIKSIT BHARAT@2047," 13-3-2024

The Workshop was organized during 9 AM to 12.30 PM on 13th March 2024. The function was presided by our esteemed Director Prof N. P. Padhy who delivered the opening address. The expert Dr. Geetha Manjunath and Mr. H. S. Jatana delivered the technical talks. The programme covered live streaming of foundation-stone laying of three semiconductor facilities by hon’ble Prime Minister Mr. Narendra Modi along with his address to nation.

A significant highlight of the seminar was the live address by Hon’ble Prime Minister Shri Narendra Modi, wherein he reiterated the government's unwavering commitment to advancing India's semiconductor industry. His speech underscored the pivotal role of semiconductor technology in driving India's technological progress and fostering innovation-led growth.

The seminar attracted a **diverse audience**, including students, and faculty members. Notable attendees included Hon'ble Director MNIT Jaipur, Prof N.P. Padhy, renowned experts in the field of semiconductor technology, Dr. H. S. Jattana and Dr. Geetha Manjunath, and participants from various sectors with a vested interest in India's technological advancement.

A total of 700+ students, and faculty members attended the seminar.

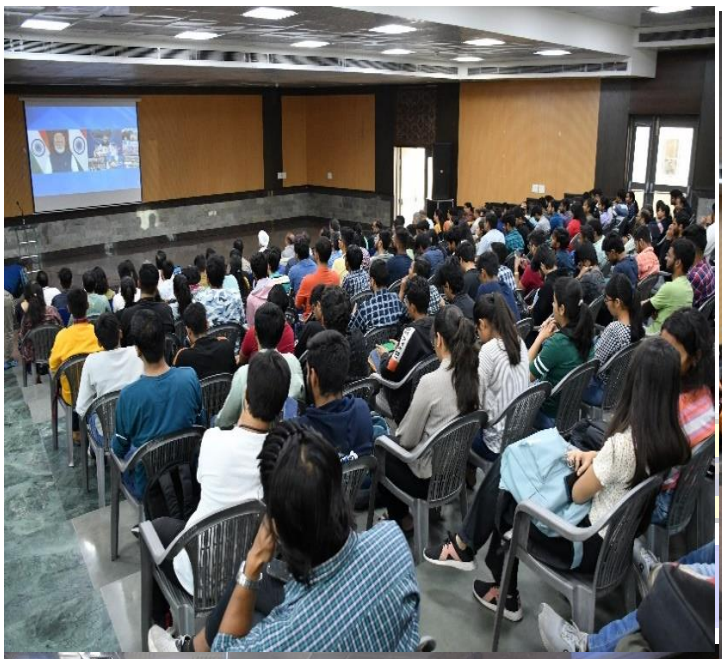
Dr. Geetha Manjunath is the Founder, CEO and CTO of NIRAMAI. She holds a PhD in Computer Science from Indian Institute of Science and management education from Kellogg’s School of

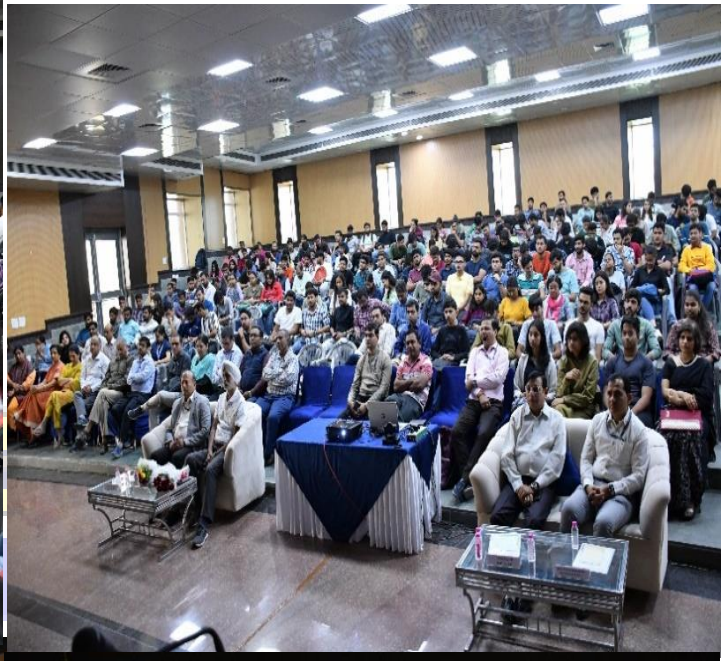
Management Chicago. She has over 25 years of experience in IT research and has led many innovative projects in Healthcare and Transportation, especially catering to Emerging Market needs. Until end of 2016, she was a Lab Director heading Data Analytics Research in Xerox India. Prior to that, she was a Principal Research Scientist at Hewlett Packard Laboratories for 17 years, and a member of the C-DAC team which built the first commercial supercomputer from India. Geetha has won many international and national recognition for her innovations and entrepreneurial work. She was awarded the CSI Gold Medal in 1991, TRS State Award, was named as one of the top 50 NASCCOM IT Innovators in 2009. She was also the winner of 2010 MIT Tech Review Grand Challenges for Technologists and BIRAC WinER Award 2018 for her Entrepreneurial Research. . She has co-authored a book on Cloud Technologies called "Moving to the Cloud". She is a Senior member of IEEE and past Chair of IEEE Computer Society, Bangalore Chapter. She is the inventor of 15 US patents with more pending grant.

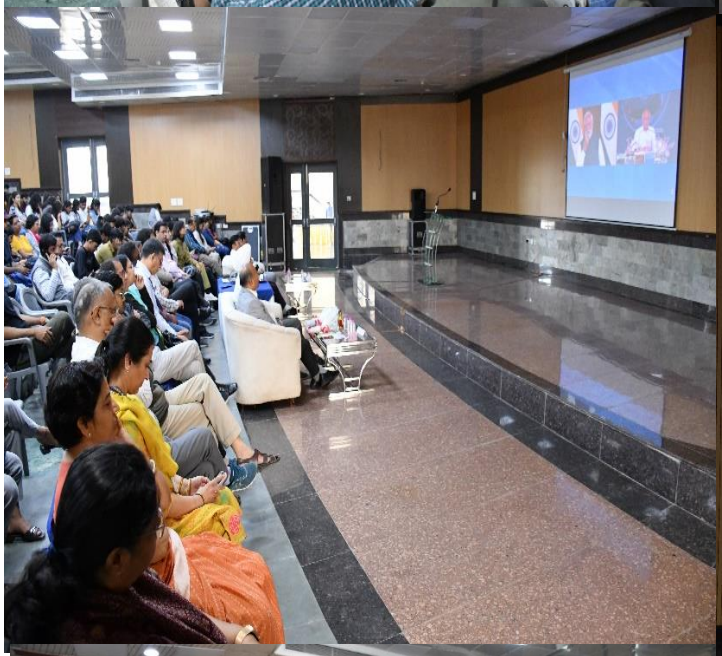
Mr. H. S. Jatana, Sci/Engr 'SG'; Group Head - Design & Process Grp; SCL /Dept of Space; Govt of India. Received his engineering education BTech (hons) from BITS Pilani and had a brief stint at CMC Delhi as Software engineer wherein he worked on Railway Computerization Project, and later joined SCL in the CMOS division.

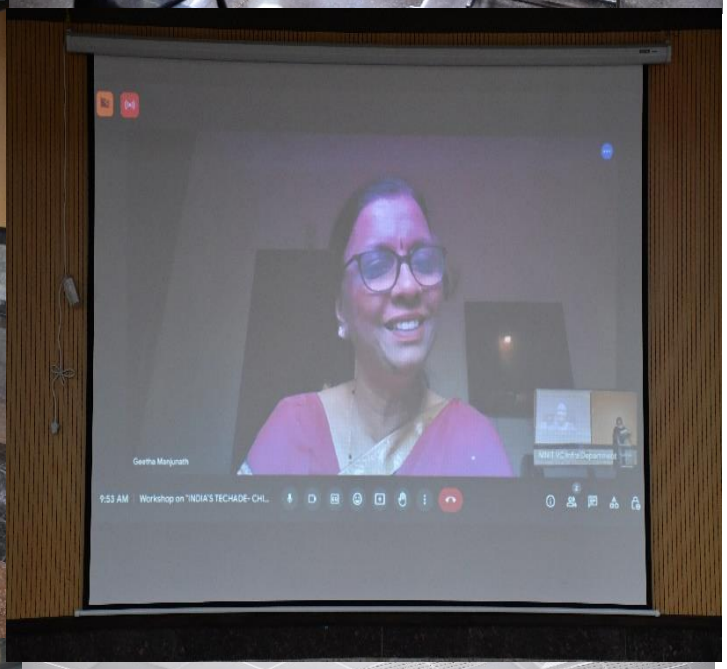
He worked at Rockwell Semiconductor, California, USA where he was involved in design of R65 series of devices. He has worked in different areas of CMOS and has vast experience on CMOS design, Device testing /, characterization, Test program development on ATE, Silicon debugging, and process Integration / porting over few technology nodes; starting from 5 μm to sub-micron nodes. He also worked at AMS Austria for ten months on deputation for porting of SCL's CMOS processes at their foundry. Presently, as Group Head at SCL / ISRO is managing four key divisions: VLSI Design, Process Development, Electro-optics devices and MEMS Design.

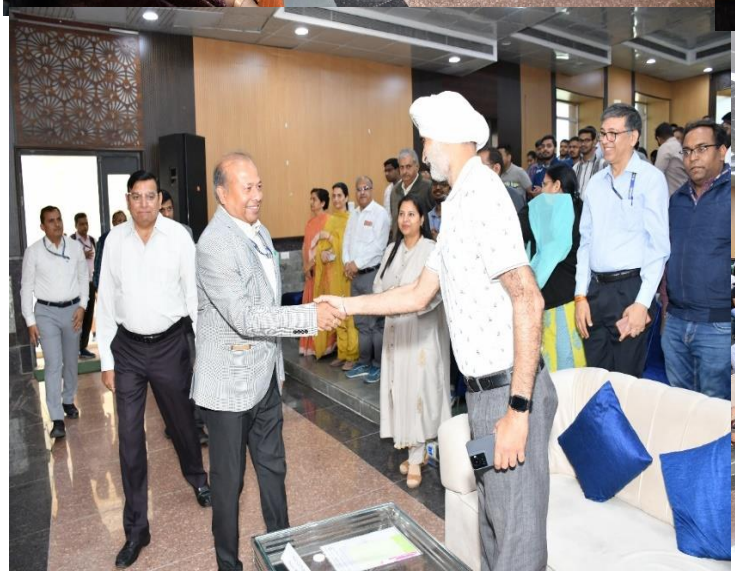
He has been instrumental in design of various ASICs and products viz, Energy meter chip, Single chip telephone, 12-bit ADC, 14-bit DAC, CMOS Imaging Sensor CIS, signal processor, SRAM, LVR, LDO' s, RAdHARD devices etc. His areas of interest are low power CMOS design, analog design in DSM regime, process enhancements / optimization in DSM era. Has initiated many new process development modules like HV, SOI, BiCMOS, CCD process technology with back thinning, III-V materials on Si for photonics etc and APS for camera application, ultra-low power circuits (bias of few nA), rail-to-rail OTAs, RHDB SRAM etc.

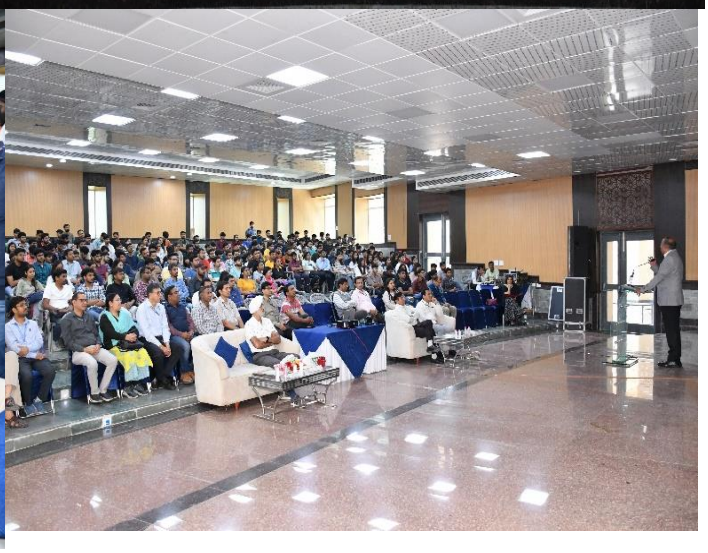


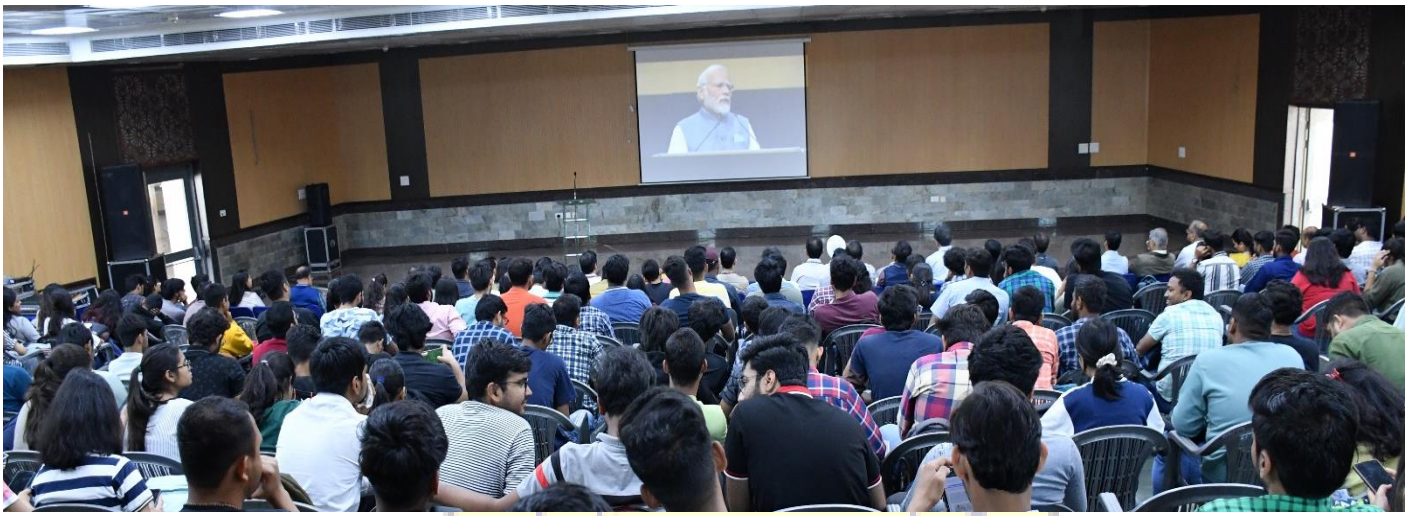





Geetha Manjunath
9:53 AM
Workshop on "INDIA'S TECHADE- CHI...







शिक्षा मंत्रालय
MINISTRY OF
EDUCATION
सत्यमेव जयते

MALAVIYA NATIONAL INSTITUTE OF TECHNOLOGY JAIPUR

A SEMINAR on INDIA'S TECHADE CHIPS FOR

VIKSIT

BHARAT@2047

DATE - 13TH MARCH 2024
VENUE - RADHAKRISHNAN HALL & ABDUL KALAM AZAD HALL AT VLTC
TIME - 9:30 AM TO 12:30 PM

EVENT HIGHLIGHTS

LIVE STREAMING OF LAYING OF FOUNDATION STONE OF

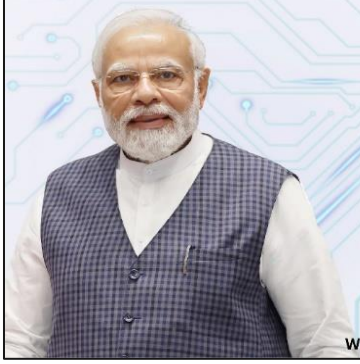
3 SEMI CONDUCTOR FACILITIES

BY HON'BLE PRIME MINISTER SHRI NARENDRA MODI

&

EXPERT TALKS

ADDRESS OF PM TO THE YOUTH



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