Master of Technology in **Embedded Systems**

Department of Electronics & Communication Engineering

Malaviya National Institute of Technology Jaipur

Subject Code	Course Title	Credit Total (L T P)
Semester 1 (Core Courses)		
ECT631	Digital System Design & FPGAs	3 (3-0-0)
ECT701	Data Structures & Algorithms	3 (3-0-0)
ECT702	Advanced Microcomputer Systems & Interfacing	3 (3-0-0)
ECT703	CAD Algorithms for Synthesis of VLSI Systems	3 (3-0-0)
ECT990	Mathematical Methods & Techniques for ECE Technologists-I*	3 (3-0-0)
ECT992	Mathematical Methods & Techniques for ECE Technologists-II*	3 (3-0-0)
ECP709	Hardware Systems Lab	2 (0-0-4)
ECP711	Software Systems lab	2 (0-0-4)
	Total Semester Credits	**19**
Semester 2 (2 + 5 electives)		
ECP712	System Design Lab	3 (0-0-6)
ECD656	Minor Project	4 (0-0-8)
	(Elective Courses)#	
ECT616	Computer Arithmetic & Micro-architecture Design	3 (3-0-0)
ECT618	Graph Algorithms & Combinatorial optimization	3 (3-0-0)
ECT622	System Level Design & Modeling	3 (3-0-0)
ECT624	VLSI Testing & Testability	3 (3-0-0)
ECT626	Formal Verification of Digital Hardware & Embedded Software	3 (3-0-0)
ECT628	Memory Design & Testing	3 (3-0-0)
ECT630	Advance Computer Architecture	3 (3-0-0)
ECT632	Embedded SoC & Cyber Physical Systems	3 (3-0-0)
ECT634	Micro-& Nano-electro-mechanical Systems (MEMS & NEMS)	3 (3-0-0)
ECT638	Design of Asynchronous Sequential Circuits	3 (3-0-0)
ECT642	FPGA's Physical Design	3 (3-0-0)
ECT648	Languages for (i) Hardware Description, (ii) Scripting and (iii) Simulation; (alternately, 1-credit each, also)	3 (3-0-0)
ECT652	RF MEMS	3 (3-0-0)
ECT654	RF Integrated Circuits	3 (3-0-0)
ECT656	Adaptive Signal Processing	3 (2-0-2)

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ECT657	VLSI Signal Processing Architectures	3 (2-0-2)
ECT662	Advanced Digital Signal & Image Processing	3 (3-0-0)
ECT690	Wireless Sensor Networks	3 (3-0-0)
ECT704	Computer vision	3 (3-0-0)
ECT706	Advanced Embedded software design	3 (3-0-0)
ECT733	Pattern Analysis & Machine intelligence	3 (3-0-0)
ECT734	Internet of Things & IIoT	3 (3-0-0)
ECT735	Probabilistic Machine Learning & AI	3 (3-0-0)
CPT602	Parallel & Distributed Systems	3 (3-0-0)
Over and Above Required Credits (Optional)		
ECT761	Special Modules in Embedded Systems Design-I	1 (1-0-0)
ECT762	Special Modules in Embedded Systems Design-II	1 (1-0-0)
ECT763	Special Modules in Embedded Systems Design-III	1 (1-0-0)
ECT764	Special Modules in Embedded Systems Design-IV	1 (1-0-0)
	Total Semester Credits	**22**
Semester 3		
ECD659	Dissertation	16(0 0 32)
	Total Semester Credits	**16**
Semester 4		
ECD660	Dissertation	16(0 0 32)
	Total Semester Credits	**16**
	Total Credits of all semesters	**73**

#The students may opt for *any course from MTech (**VLSI**) and selected courses form other MTech streams* in the Institute/department on recommendation of supervisor

*****Only one course out of ECT990 or ECT992 shall be opted by a student

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Program: M Tech in Embedded System	Department: Electronics & Communication Engineering
Course Code: ECT631	Course Name: Digital System Design & FPGAs
Credit: 3	L-T-P: 3-0-0
Pre-requisite Course:	
Co-requisite Course:	

Syllabus:

Sequential Logic Design-Introduction, Basic bistable Memory Devices, additional bistable devices, reduced characteristics and excitation table for bistable devices.

Synchronous Sequential Logic Circuit Design- Introduction, Moore, Mealy and Mixed type Synchronous State Machines. Synchronous sequential design of Moore, Melay machines,

Algorithmic State Machine- An Algorithm with inputs, digital solution, Implementation of traffic light controller, ASM charts, Design Procedure for ASMs.

Data path and Control design.

Introduction to VHDL/Verilog- Data types, Concurrent statements, sequential statements, behavioral modeling. Introduction to programmable logic devices- PALs, PLDs, CPLDs and FPGAs.

FPGA mapping of combinational & sequential designs

References:

1. Digital System Design, Ercegovac, Wiley.
2. Richard S. Sandige, *Modern Digital Design,* McGraw-Hill, 1990.
3. Zvi Kohavi, Switching and Finite Automata Theory, Tata McGraw-Hill.
4. Navabi. Analysis and modeling of digital systems. McGraw Hill, 1998.
5. Perry. Modeling with VHDL. McGraw Hill, 1994.
6. Navabi. Verilog Digital Design. McGraw Hill, 2007.
7. Fundamentals of Digital Logic with Verilog Design, Stephen Brown and Zvonko Vranesic, McGraw Hill, 2002.

Course Outcomes:

CO1. To be able to apply the basic design principles of sequential logic systems. (Cognitive- Applying)

CO2. To understand the design concepts of synchronous state machines in Moore and Mealy architectures. (Cognitive- understanding)

CO3. To analyze & design data path, control path design and various programmable devices (Skills- Create)

CO4. To be able to implement a digital system using HDLs (Skills- Evaluate)

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Program: M Tech in Embedded System	Department: Electronics & Communication Engineering
Course Code: ECT701	**Course Name: Data Structure & Algorithms**
Credit: 3	**L-T-P: 3-0-0**
Pre-requisite Course:	
Co-requisite Course:	

Syllabus:

Introduction to data structures. Static and dynamic aspects of memory allocation. Recursion and its applications. Introduction to complexity analysis, measure and representation.

Algorithms for searching and Sorting, Non-recursive and recursive implementation of searching. Non-recursive and recursive sorting algorithms.

Creation and manipulation of data structures: arrays, stacks, queues and linked lists with static and dynamic memory allocation. Applications.

Creation, manipulation and analysis of trees. Binary search tree algorithms.

Graph problems: Shortest path implementation. Introduction to Max Flow-Min Cut and travelling salesman problem.

Introduction to height balanced trees: AVL and B Trees.

References:

1. Rivest, Cormen, Introduction to Algorithms, MIT Press
2. Horowitz and Sahni: Data Structure in C++ , Glagotia
3. Ellis Horowitz, Sartaj Sahni, Fundamentals of Data Structures
4. Aaron M. Tenenbaum, Y. Langsam, Moshe J. Augenstein, Data Structures Using C

Course Outcomes:

CO1. To impart the basic concepts of data structures and algorithms.

CO2. To understand concepts about searching and sorting techniques.

CO3. To understand basic concepts about stacks, queues, lists, trees, and graphs.

CO4. To understanding about writing algorithms and step by step approach in solving problems with the help of fundamental data structures.

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Program: M Tech in Embedded System	Department: Electronics & Communication Engineering
Course Code: ECT702	Course Name: Advanced Microcomputer Systems & Interfacing
Credit: 3	L-T-P: 3- 0- 0
Pre-requisite Course:	
Co-requisite Course:	

Syllabus:

Introduction;

Processor-processor (Intel/ARM) and micro controller (Intel/ARM), assembly language programming,

Interfacing methods-protocols, synchronization, parallel I/O, serial I/O, Memory interfacing, Digital/Analog interfacing, high speed I/O interfacing, data acquisition systems, CAN, I2C, USB, ESSI (Enhanced Synchronous Serial Interface) protocols; General Purpose Input/Output (GPIO)

Interrupt Synchronization & Timing generation- Features of interrupts, interrupt vectors & priority, polling, priority algorithms; frequency measurement, frequency and period conversion.

Miscellaneous- Serial and parallel port interfaces; State machine & concurrent process models. System examples-camera etc; Debugging: JTAG, ISP, BDM Port, BITP, and DB9 ports.

References:

1. Jonathan W. Valvano, Embedded Microcomputer Systems: Real-Time Interfacing, Brookes/Cole, Pacific Grove, 2000.
2. Douglas V. Hall , Microprocessors and interfacing, McGraw Hills,
3. K.Ayala, The 8051 Microcontroller, Thompsons, Mazidi,Naimi, Naimi , avr microcontroller and embedded system, pearsons.
4. David A. Patterson and John L. Hennessy, Computer Organization and design ARM ed.,Morgan Kaufmann,
5. F. Vahid & T. Givargis, Embedded System Design, Wiley.
6. Wolf, W., Computers as Components: Principles of Embedded Computing System Design, Morgan Kaufmann, San Francisco, 2001.
7. Furber, S., ARM: system-on-chip architecture, 2nd Edition, Addison-Wesley, London, 2000.
8. Hayes, J. P., Computer Architecture and Organization, 3rd Edition, McGraw-Hill
9. Manuals- Intel 32/64 Architectures , ARM manual - 32/64-bit architecture, Intel 8051 and ATmega328P datasheet

Course outcomes:

CO1. To Understand the 16,32,64-bit processors ISA (CISC and RISC)
CO2. To understand the language and use of micro controller (ARM/Atmega 328)
CO3. To understand different I/O interface protocols and write programs for ARM interfaces
CO4. To understand memory and different transducers and interfacing
CO5. To write assembly programmes interfacing and design issues of embedded system(analytically and design issues)

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Program: M Tech in Embedded System	Department: Electronics & Communication Engineering
Course Code: ECT703	Course Name: CAD Algorithms for Synthesis of VLSI Systems
Credit: 3	L-T-P: 3-0-0
Pre-requisite Course:	
Co-requisite Course:	

Syllabus:

Unit 1: Introduction to CAD Algorithms

Role of CAD in digital system design, levels of design, modelling & description and support of languages, RTL, gate and system level synthesis; Technological alternatives and technology mapping

Unit 2: CAD Tools for synthesis

CAD tools for synthesis, optimization, simulation and verification of design at various levels as well as for special realizations and structures such as micro-programmes, PLAs, gate arrays etc. Technology mapping for FPGAs. Low power issues in high level synthesis and logic synthesis.

Unit 3: Architectural-Level Synthesis and Optimization

Architectural Synthesis, Scheduling, Data path synthesis and control unit synthesis, scheduling algorithm, Resource Sharing and Binding

Unit 4: Logic-Level Synthesis and Optimization

Two-Level Combinational Logic Optimization, Multiple-Level Combinational Logic Optimization, Sequential Logic Optimization

Unit 5: CAD Algorithms for VLSI Physical Design

Introduction to VLSI Physical Design flow. Circuit partitioning, placement and routing algorithms. Design Rule-verification, Circuit Compaction; Circuit Extraction and post layout simulation. FPGA design flow- partitioning, placement and routing algorithms. Deep sub-micron issues; interconnects modeling and synthesis.

References:

1. G. D. Micheli. Synthesis and optimization of digital systems.
2. Dutt, N. D. and Gajski, D. D. High level synthesis, Kluwer, 2000.
3. T. H. Cormen, C. E. Leiserson and R. L. Rivest, “Introduction to Algorithms,” McGraw-Hill, 1990.
4. N. Deo, Graph Theory, PH India.
5. Sait, S. M. and Youssef, H. VLSI Physical design automation. IEEE press, 1995.
6. Sherwani, N. VLSI physical design automation. Kluwer, 1999.

Course Outcomes:

CO1. Is able to grasp various operations on graphs, clique, coloring, partitioning etc
CO2. & apply graph algorithms and its applications into Boolean function representation (Knowledge)
CO3. Is able to grasp graph models for architecture representation (Knowledge)
CO4. Is able to analyse & implement two level/Multilevel/ sequential logic synthesis algorithms
CO5. (approximate & exact algorithms) (skills)
CO6. Is able to analyze & implement library binding algorithms- FSM equivalence & optimization (skills)
CO7. To able to grasp core concept of VLSI Physical Design. (Knowledge)

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Program: M Tech (ECE)	Department: Electronics & Communication Engineering
Course Code: ECT990	Course Name: Mathematical Methods and techniques for Electronics & Communication Technologists-I
Credit: 3	L-T-P: 3-0-0
Pre-requisite Course:	
Co-requisite Course:	

Syllabus:

Advancements in Transforms: Discrete Fourier Transform, FFT, Short time Fourier Transform (STFT), Multi Resolution Analysis, Wavelet Transform, Continuous Wavelet Transform (CWT), Inverse CWT, Discrete Wavelet Transform, Sub-band coding and implementation of DWT, Applications (signal and image compression, de-noising, detection of discontinuous and breakdown points in signals), Discrete Cosine Transform, Stockwell-transform, Frequency selective filtering with wavelet and S-transform.

Modelling: Direct Modeling (identification), Inverse Modeling(Equalization), Classification and Clustering, Prediction/Forecasting, Auto regressive models (AR, MA, ARMA).

Optimization: Problem formulation, Linear Programming Problems, Solution by Graphical Methods, Symmetric Dual Problems, Slack and Surplus Variables, Simplex Method, Convex- Concave Problems.

Data Mining Techniques: Higher Order Statistics, Principal Component Analysis, Linear Discriminant Analysis, Independent Component Analysis

References:

1. Digital Signal Processing: Principles, Algorithms, and Applications 4 Edition, Author: John G. Proakis, Dimitris G Manolakis Publisher: Pearson.
2. Wavelets and Signal Processing, Author: Hans-Georg Stark, Publisher: Springer
3. The Wavelet Tutorial : The Engineer's Ultimate Guide to Wavelet Analysis, Author : Robi Polikar, University of Rowan : Online : http://users.rowan.edu/~polikar/WTtutorial.html
4. Stockwell, Robert Glenn, Lalu Mansinha, and R. P. Lowe. "Localization of the complex spectrum: the S transform." IEEE Transactions on Signal Processing 44.4 (1996): 998-1001.
5. Engineering Optimization: Theory and Practice, Third Edition SINGIRESU S. RAO, New Age Publishers
6. Data Mining - Concepts and Techniques, Authors : Jain Pei, Jiawei Han, Micheline Kamber, Publisher : Elsevier

Course Outcomes:

CO1.To learn the advancement in transforms
CO2.To understand the mathematical modeling and optimization techniques.
CO3.To learn the data mining techniques
CO4.To explore the engineering applications of the mathematical techniques.
CO5.To develop MATLAB and other programming skills for the mathematical techniques realization.

DPGC Convener Head, ECE SPGB Chairman

Program: M Tech in Embedded System	Department: Electronics & Communication Engineering
Course Code: ECT992	Course Name: Mathematical Methods and techniques for Electronics & Communication Technologists-II
Credit: 3	L-T-P: 3-0-0
Pre-requisite Course:	
Co-requisite Course:	

Syllabus:

[The following contents intend to cover implicit application to and exemplification through ECE problems in Electronic systems/Cognitive-systems domain such as reduced order polynomials, order reduction of a transfer function, sparse matrix based solution of large systems, discrete structures, implementation of search algorithms for design space exploration, and computer arithmetic implementation along with probabilistic reasoning for AI]

A. (i) (a) Large Matrix analysis and large Eigen value problem– Groups, fields and rings; vector spaces; basis & dimensions; canonical forms; inner product spaces- orthogonalization, Gram-Schmidt orthogonalization, unitary operators, change of orthonormal basis, diagonalization; (b) Eigenvalues & eigen vectors- Gerschghorin theorem, iterative method, Sturm sequence, QR method, introduction to large Eigen value problems. 08 Hrs.

(ii) Reduced order modelling of systems- Taylor's polynomial, least square approximation, Chebyshev series/polynomial, splines, Pade & rational approximation 04 Hrs.

B. Discrete Structures, graphs, algorithms & Combinatorial optimization- counting methods, algorithm analysis, graph algorithms, dynamic algorithms, randomized algorithms, probabilistic algorithms, combinatorial optimization16 Hrs.

C. (i) Number theory & computer arithmetic- unconventional number systems, residue number system, logarithmic number system, Chinese remainder theorem; fast evaluation of elementary & transcendental arithmetic functions. 06 Hrs.

(ii) Preface to AI- first order logic & inferencing, uncertainty, probabilistic reasoning systems, making decisions under uncertainty; **08 Hrs.**

Suggested references (not limited to)-

1. Schaum's outline on Linear Algebra, McGraw Hill
2. Topics in Algebra, I. N. Herstein, Wiley.
3. Gerald, C F; Wheatley P O; Applied Numerical Analysis, Pearson, 2017
4. Theory and Applications of Numerical Analysis, G. M. Phillips, Peter J. Taylor, Academic press
5. Advanced Model Order Reduction Techniques in VLSI Design, Sheldon Tan, Lei He, Cambridge Univ. Press, 2007.
6. Cormen, Rivest, Leiserson, Introduction to Algorithms, PHI
7. Combinatorial optimization, Papadimitriou and Steiglitz, PHI (I)
8. Russel and Norvig- Artificial Intelligence: A Modern Approach, Pearson, 3rd Ed. 2017
9. Israel Koren, Computer Arithmetic- Academic Press
10. Model Order Reduction: Theory, Research Aspects and Applications edited by W. H. A. Schilders, Henk A. Van Der Vorst, Joost Rommes, Springer.
11. Discrete Structures, Schaum outline

Further references

1. MODEL ORDER REDUCTION TECHNIQUES WITH APPLICATIONS IN ELECTRICAL ENGINEERING**,** Luigi FORTUNA, Guiseppe NUNNARI, Antonio GALLO, Springer, 1992.
2. Y. Saad, Numerical methods for large Eigenvalue problems, www.umn.edu
3. Matrix Analysis & linear algebra, Meyer, SIAM
4. H. A. van der Vorst, Iterative methods for large linear systems, citeseerx.ist.psu.edu
5. Cheng et al, Symbolic analysis and reductions of VLSI circuits, Springer, 2005

Course Outcomes:

CO1. Is able to grasp core concepts, basic tenets of linear algebraic structures- groups, fields and rings;vector

spaces (knowledge)

CO2. Is able to grasp features, properties and operations on vector spaces- orthogonalization, change of basis, diagonalization (knowledge)

CO3. Is able to learn & apply problem solving for computing eigen values and eigen vectoraetc. (Thinking, skills)

CO4. Is able to demonstrate application of algorithms (Gerschgorin, Sturm sequence method, QR method) for eigen value computation/estimation and MATLAB validation(skills)

CO5. Is able to describe algorithms for function approximation (rational, Chebychev, Pade etc.) using MATLAB (skills)

CO6. Develops appreciation for combinatorial optimization algorithms, AI probabilistic approaches & implements through MATLAB/C++ (skills)

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Program: M Tech in Embedded System	Department: Electronics & Communication Engineering
Course Code: ECP709	**Course Name: Hardware Systems Lab**
Credit: 2	**L-T-P: 0-0-4**
Pre-requisite Course:	
Co-requisite Course:	

Syllabus:

Problem-set for algorithm implementation:

Boolean algebraic formulations

a. Covering algorithm- Brach & bound
b. ROBDD computation
c. Operation between ROBDDs: '+', '.'

Graph based optimization

a. Two consideration each
b. Two consideration each
c. Graph coloring
d. Clique partitioning
e. Edge covering
f. Vertex covering
g. Independent set finding

List scheduling

a. Latency constrained resource minimization
b. Resource constrained latency minimization
c. Path based scheduling
d. Pipelined data-path scheduling
e. Hu's multiprocessor scheduling

Allocation & binding

a. FU binding
    a. Coloring
    b. Clique finding
    c. Left edge based binding
b. Storage unit binding
    a. Coloring
    b. Clique finding
    c. Left edge based binding
c. Interconnect binding
    a. Coloring

Clique finding edge based binding

Course Outcomes:

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Program: M Tech in Embedded System	Department: Electronics & Communication Engineering
Course Code: ECP711	**Course Name: Software Systems Lab**
Credit: 2	**L-T-P: 0-0-4**
Pre-requisite Course:	
Co-requisite Course:	

Syllabus:

1. Design of software
    a) Assembly language programming
    b) Device drivers writing
    c) Object oriented interfacing,
    d) Debugging
2. Interfacing methods
3. Analog interfacing, data acquisition systems (board based)

References:

Course Outcomes:

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Program: M Tech in Embedded System	Department: Electronics & Communication Engineering
Course Code: ECP712	**Course Name: System Design Lab**
Credit: 3	**L-T-P: 0-0-6**
Pre-requisite Course:	
Co-requisite Course:	

Syllabus:

Group Application/Problems:

1. A-1 Layout Design- (i) Full adder, D-FF ; & (ii) synthesis of combinational & Sequential Components- 4-bit adder, 4-bit shift register, sequence detector ("1010")
2. A-2 Layout synthesis of already designed (1st Odd Semester) Data Path & Control for an arithmetic/logic application. Synthesis Using SYNOPSYS/CADENCE tool

Individual Application/Problems:

1. GCD-computer (4-bit)
2. Booth multiplier (4-bit)
3. 4-pt FFT
4. 4-pt IFFT
5. CORDIC for SinΘ/CosΘ
6. CORDIC for Sin-1Θ/Cos-1Θ
7. Non-Linear function exp(-2.5)/Sin 1.45/ Cos3.1/Sinh2.5/ Cosh3.2/log-natural
8. Find Average of Floating Point Numbers in Array of Size 16/32/64/128
9. For pseudo exhaustive TPG set T for BIST, follow the theorem concerning logical segmentation, which relates n (inputs), k (subspaces of size k among n), w (weight of n-tuple). Indicate w as well as |Tc| for different c; and n=20, k=3. Take example circuits/sub-systems for implementing the scheme & generating/applying random test patterns.
10. A circuit implementing f=xy+yz is to be tested using the syndrome-test method. Show that the faults z s-a-0 and z s- a-1 are not detected, while all other single stuck-at faults are detected. Arrange for experimental setup for all such testable as well as non-testable faults.
11. In a shift register polynomial division method of compression, a type 2 LFSR with P*(x)=1+x2+x4+x5 is to be used for input sequence 1 1 1 1 0 1 0 1 (8 bits). Compute signature for the input sequence. Indicate at least one more input sequence, which would alias the given sequence. Arrange for experimental setup for verifying your design.

References:

Course Outcomes:

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